

5.5 GHz – 13.5 GHz Phase Locked Loop IP Block

General Description

The PLL13G is an ultra-low power phase locked loop (PLL) intellectual property (IP) block.

The PLL13G features a very small area footprint, with exceptional jitter performance in its power/area class and flexible programmability, making this IP ideal for a wide range of general purpose clocking and specialized applications.

The PLL13G is optimized for use in high-performance data converters with wide input bandwidths and/or high sampling rates and advanced interfaces such as PCIe.

The advanced IP block has been designed and verified in TSMC 130nm process.

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Key Features

- ◆ Input Frequency: ~40MHz
- ◆ Output Frequency: 5.5-13.5 GHz
- ◆ RMS Jitter: <350 fs
- ◆ Supply Voltage: 1.2 V
- ◆ Power: 50.88 mW
- ◆ LC-Tank
- ◆ TSMC 130nm Process
- ◆ Area: 0.75 mm²
- ◆ Radiation-tolerant Version Available:
PLL13GRH

Applications

- ◆ High Speed Interfaces
- ◆ High Speed Test Instruments
- ◆ 5G Cellular Base Stations
- ◆ Communications and Networking
 - ◆ Microwave Receivers
 - ◆ Radar and Satellite Communications
- ◆ Sensor/Detector Readout Applications
- ◆ Automotive Applications